Lab 6 Victor Yuan

Introduction: October 6, 2012

In this lab a Boolean expression was derived from a 1:2 demultiplexer function table. Then the expression was implemented into Verilog to test out if the expression was correct. Finally it was implemented into hardware.

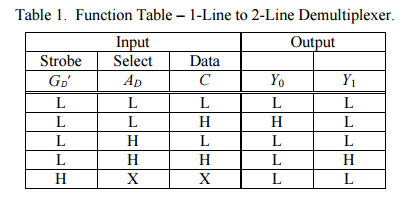
Team Member Responsibilities:

This lab was done alone.

Materials:

ELENCO kit CMOS logic gates assorted wires

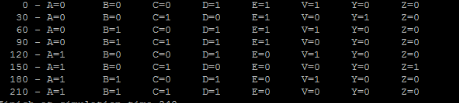
Procedure:



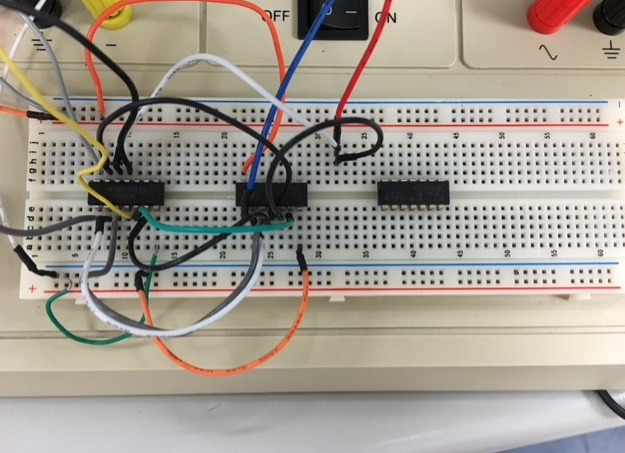
First, derive a Boolean expression from the table above, then simplify it as much as possible. Once the Boolean expression has been derived open up PUTTY and make a Verilog file in a folder/directory. The Verilog file should look like this:



Save the file then execute the program by typing “Verilog (insert filename here).v” the results should look like this:



Check the input outputs with the input output of the original table, if they match then proceed to hardware implementation.



QUESTIONS:

I. Experiment:

1. How do the Verilog simulation truth-table and hardware implementation truthtable

for the 1:2 demultiplexer compare?

They are the same with the only difference of being able to see the time delays between the switches on the Verilog truth table.

2. Does your design correctly implement the function table for a 1:2 demultiplexer

given in Table 1?

Yes my design correctly implemented the function table although it took a few tries from a faulty wiring issue.

II. Conclusions:

1. Discuss how you could build a 1:16 demultiplexer using 1:4 demultiplexers.

To build a 1:16 demultiplexer I would need to use each gate on the 1:4 demultiplexer four times. Each time would have to be a different gate aswell.